PUN-ENCODED CM85A CIRCUIT SCHEMATICS
William Bricken
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Structural Varieties

Optimization

- SCHEMATIC 1: Two-level Logic (PLD)
- SCHEMATIC 2: Multilevel Benchmark Circuit (cm85a)
- SCHEMATIC 3: Suppress Inverters
- SCHEMATIC 4: Remove Redundancy
- SCHEMATIC 5: Reduce Reconvergence
- SCHEMATIC 6a: Increase Fanin (poor choice)
- SCHEMATIC 6b: Increase Fanin (good choice)
- SCHEMATIC 7a: Enhance Testability (poor choice)
- SCHEMATIC 7b: Enhance Testability (good choice)

Design Constraints

- SCHEMATIC 8: Reduce Critical Path (6 gates)
- SCHEMATIC 9: Pipeline (3 two-input gates)
- SCHEMATIC 10a: Map to Specific Library (poor choice)
- SCHEMATIC 10b: Map to Specific Library (good choice)
- SCHEMATIC 11: Three-level Logic
- SCHEMATIC 12: Map to NAND Gates
- SCHEMATIC 13: Map to FPGA (4-LUTs)
- SCHEMATIC 14: Binary Decision Diagram

Hierarchical Abstraction

- SCHEMATIC 15: Abstract Low-level Components
- SCHEMATIC 16: Abstract for Component Connectivity
- SCHEMATIC 17: Abstract for Sequential Structure
- SCHEMATIC 18: Abstract for Parallel Structure
- SCHEMATIC 19: Abstract for Output Structure
- SCHEMATIC 20a: Abstract Bit-width (recursive)
- SCHEMATIC 20b: Abstract Bit-width (enables)
- SCHEMATIC 20c: Abstract Bit-width (enables, recursive)

BTC Hardware Models

- SCHEMATIC 21: Distinction Network I
- SCHEMATIC 22: Distinction Network II
- SCHEMATIC 23a: Occlusion Array (Dnet 21)
- SCHEMATIC 23b: Occlusion Array (Dnet 22)
- SCHEMATIC 23c: Occlusion Array (two-level Dnet)
- SCHEMATIC 23d: Occlusion Array (raw multilevel benchmark)
- SCHEMATIC 23e: Occlusion Array (clean multilevel benchmark)
- SCHEMATIC 24a: Comesh (multilevel)
- SCHEMATIC 24b: Comesh (two-level)
- SCHEMATIC 25: Bit-stream Simulator

UPDATE

- SCHEMATIC 26: Semantic Optimization, Remove EqualTo
- SCHEMATIC 27: Semantic Optimization, Remove LessThan
- SCHEMATIC 28: Map to high fan-in NOR gates
- SCHEMATIC 29: Fan-in and fan-out constraints on NOR gates
- SCHEMATIC 30: Fan-out of three constraint
- SCHEMATIC 31: Map to MUX gates
- SCHEMATIC 32: Homogeneous graph
- SCHEMATIC 33: 3D logic blocks
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J → Equal
I → Greater
K → Less

A0
B0

J
I
A0
B0

N bit magnitude comparator

Greater
Equal
Less
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Input values: 
((a 0) (b 0) (c 1) (d 1) (e 1) (f 0) (g 1) (h 0) (i 0) (j 1) (k 0))

Output #1: 
(((j )((a (b))(b (a))))((d (c ))(d (d ))(e (f ))(f (a ))(g (b))(b (g ))))

Output #2: 
(((j )((g (h))((b (g ))((e (f ))(f (a ))(a (b))(d (c ))))))))

Output #3: 
(((k )((j )((h (g ))((g (h))((f (e ))(e (f ))(d (c ))(b (a)(c (d ))))))))

BIT STREAM INPUT

111001110011100110100111000111001001100011110001100011101001110000000000000

Single Pass Evaluation

0

1111100111101111001110100111001100110011100110011100110011001110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111001100111001100110011100110011100110011001110011001110011001100111
SCHEMATIC 26 & 27: Semantic Optimization

SEMANTIC OPTIMIZATION TO DELETE THE EQUALTO BRANCH

SEMANTIC OPTIMIZATION TO DELETE THE LESSTHAN BRANCH
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EqualTo

GreaterThan

LessThan